```
L1          5789 S ((EEPROM OR FLASH) (2A) MEMORY)
L2        138440 S (VOLT? OR THRESHOLD) (2A) (LEVEL# OR VALUE#)
L3           353 S L1 (P) L2
L4           274 S L3 AND (395 OR 365 OR 371 OR 711)/CLAS
L5           683 S L1/TI,AB
L6           121 S L4 AND L5
L7         39097 S L2/AB,CLM
L8            58 S L6 AND L7

=> D 1-58
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2. 5,721,702, Feb. 24, 1998, Reference voltage generator using **flash memory** cells; Michael S. Briner, **365/185.21, 185.3, 189.09** [IMAGE AVAILABLE]

3. 5,706,239, Jan. 6, 1998, Rechargeable SRAM/flash PCMCIA card; Wieslaw Brys, **365/226, 185.33, 227, 228** [IMAGE AVAILABLE]

4. 5,694,366, Dec. 2, 1997, OP amp circuit with variable resistance and memory system including same; Christophe J. Chevallier, et al., **365/207**; 330/86, 282; **365/208** [IMAGE AVAILABLE]

5. 5,694,360, Dec. 2, 1997, Write to flash EEPROM built in microcomputer; Yuichi Iizuka, et al., **365/185.33, 185.18, 189.09, 226** [IMAGE AVAILABLE]

6. 5,675,537, Oct. 7, 1997, Erase method for page mode multiple bits-per-cell flash EEPROM; Colin Stewart Bill, et al., **365/185.22, 185.03, 185.12, 185.25, 185.29, 185.3** [IMAGE AVAILABLE]

7. 5,673,223, Sep. 30, 1997, Nonvolatile semiconductor memory device with multiple word line voltage generators; Jong-Wook Park, **365/185.17, 185.11, 185.13, 230.06** [IMAGE AVAILABLE]

8. 5,666,307, Sep. 9, 1997, PMOS **flash memory** cell capable of multi-**level threshold voltage** storage; Shang-De Ted Chang, **365/185.03, 185.19, 185.26, 185.33** [IMAGE AVAILABLE]

9. 5,642,310, Jun. 24, 1997, System and method for controlling source current and voltage during **flash memory** erase operations; Paul Jei-zen Song, **365/185.29, 185.27, 189.09** [IMAGE AVAILABLE]

10. 5,638,327, Jun. 10, 1997, **Flash-EEPROM memory** array and method for biasing the same; Marco Dallabora, et al., **365/185.15, 104, 185.02, 185.12, 185.18, 185.28, 185.29** [IMAGE AVAILABLE]

11. 5,621,685, Apr. 15, 1997, Programmable power generation circuit for **flash EEPROM memory** systems; Raul-Adrian Cernea, et al., **365/185.18, 185.33** [IMAGE AVAILABLE]

12. 5,619,452, Apr. 8, 1997, Semiconductor disk device with a constant data-writing time period; Shigenori Miyauchi, **365/185.29, 185.11, 185.2, 185.33**; **711/103** [IMAGE AVAILABLE]

13. 5,619,450, Apr. 8, 1997, Drive circuit for **flash memory** with improved erasability; Tetsuji Takeguchi, **365/185.23**; 327/434; **365/185.26, 185.27, 189.09, 189.11** [IMAGE AVAILABLE]

14. 5,615,154, Mar. 25, 1997, **Flash memory** device having erase verification; Shigekazu Yamada, **365/185.22, 185.29, 218**

[IMAGE AVAILABLE]

15. 5,610,861, Mar. 11, [redacted]7, **Flash memory** device; Hyun S. Si[redacted] **365/185.24, 185.12, 185.22, 201** [IMAGE AVAILABLE]

16. 5,600,592, Feb. 4, 1997, Nonvolatile semiconductor memory device having a word line to which a negative voltage is applied; Shigeru Atsumi, et al., **365/185.18, 185.23, 185.26, 185.27, 185.29, 189.09** [IMAGE AVAILABLE]

17. 5,594,691, Jan. 14, 1997, Address transition detection sensing interface for **flash memory** having multi-bit cells; Amir Bashir, **365/185.03, 185.21, 189.05, 189.07, 203, 207, 210, 233.5** [IMAGE AVAILABLE]

18. 5,594,686, Jan. 14, 1997, Method and apparatus for protecting data stored in **flash memory**; Peter K. Hazen, et al., **365/185.04, 185.33, 226, 228** [IMAGE AVAILABLE]

19. 5,594,685, Jan. 14, 1997, Method for programming a single EPROM or **flash memory** cell to store multiple bits of data that utilizes a punchthrough current; Albert Bergemont, et al., **365/185.03, 185.18, 185.27** [IMAGE AVAILABLE]

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22. 5,581,503, Dec. 3, 1996, Data line disturbance free **memory** block divided **flash memory** and microcomputer having **flash memory** therein; Kiyoshi Matsubara, et al., **365/185.33, 185.11, 185.14, 218** [IMAGE AVAILABLE]

23. 5,579,262, Nov. 26, 1996, Program verify and erase verify control circuit for EPROM/flash; Paul J. Song, **365/185.22, 185.19** [IMAGE AVAILABLE]

24. 5,579,261, Nov. 26, 1996, Reduced column leakage during programming for a **flash memory** array; Nader Radjy, et al., **365/185.33, 185.18, 185.3** [IMAGE AVAILABLE]

25. 5,574,850, Nov. 12, 1996, Circuitry and method for reconfiguring a **flash memory**; Mickey L. Fandrich, **395/182.03** [IMAGE AVAILABLE]

26. 5,568,424, Oct. 22, 1996, Programmable power generation circuit for **flash EEPROM memory** systems; Raul-Adrian Cernea, et al., **365/185.33, 185.18, 226** [IMAGE AVAILABLE]

27. 5,563,825, Oct. 8, 1996, Programmable power generation circuit for **flash eeprom memory** systems; Raul-Adrian Cernea, et al., **365/185.18**; 327/536; **365/185.23, 185.33, 189.09, 226** [IMAGE AVAILABLE]

28. 5,559,717, Sep. 24, 1996, High precision voltage detector utilizing **flash EEPROM memory** cells; Kerry Tedrow, et al., 364/483; **365/189.07** [IMAGE AVAILABLE]

29. 5,537,358, Jul. 16, 1996, **Flash memory** having adaptive sensing and method; Vincent L. Fong, **365/218, 185.29, 185.33** [IMAGE AVAILABLE]

30. 5,517,138, May 14, 1996, Dual row selection using multiplexed tri-level decoder; Robert L. Baltar, et al., 326/105, 10, 106; **365/200, 230.06** [IMAGE AVAILABLE]

31. 5,508,971, Apr. 16, 1996, Programmable power generation circuit for **flash EEPROM memory** systems; Raul-Adrian Cernea, et al., **365/185.23, 185.14, 185.18, 189.09, 226** [IMAGE AVAILABLE]

32. 5,455,800, Oct. 3, 1995, Apparatus and a method for improving the program and erase performance of a **flash EEPROM memory** array; Steven E. Wells, et al., **365/218, 185.26, 189.09** [IMAGE AVAILABLE]

33. 5,455,794, Oct. 3, 1995, Method and apparatus for controlling the output current provided by a charge pump circuit; Jahanshir J. Javanifard, et al., **365/185.18, 226, 230.06** [IMAGE AVAILABLE]

34. 5,448,712, Sep. 5, 1995, Circuitry and method for programming and erasing a non-volatile semiconductor memory; Virgil N. Kynett, et al., **711/103; 365/218** [IMAGE AVAILABLE]

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36. 5,438,542, Aug. 1, 1995, Nonvolatile semiconductor memory device; Shigeru Atsumi, et al., **365/182**; 257/314, 371; **365/185.18, 185.23, 185.26, 185.27, 185.33, 189.04, 218, 226** [IMAGE AVAILABLE]

37. 5,414,669, May 9, 1995, Method and apparatus for programming and erasing **flash EEPROM memory** arrays utilizing a charge pump circuit; Kerry D. Tedrow, et al., **365/226, 185.29, 189.09** [IMAGE AVAILABLE]

38. 5,410,511, Apr. 25, 1995, Methods of controlling the erasing and writing of information in **flash memory**; Junji Michiyama, **365/185.22, 185.11, 185.12, 185.33, 189.11, 230.06** [IMAGE AVAILABLE]

39. 5,408,429, Apr. 18, 1995, Method of altering a non-volatile semiconductor memory device; Kikuzo Sawada, **365/185.12, 185.18, 185.26, 185.27, 185.33** [IMAGE AVAILABLE]

40. 5,377,147, Dec. 27, 1994, Method and circuitry for preconditioning shorted rows in a nonvolatile semiconductor memory incorporating row redundancy; Amit Merchant, et al., **365/185.09, 49, 185.12, 185.21, 185.22, 185.24, 185.33; 371/10.3** [IMAGE AVAILABLE]

41. 5,371,709, Dec. 6, 1994, Power management system for serial EEPROM device; Richard J. Fisher, et al., **365/226, 227** [IMAGE AVAILABLE]

42. 5,355,347, Oct. 11, 1994, Single transistor per cell **EEPROM memory** device with bit line sector page programming; Dumitru Cioaca, **365/230.08, 185.13, 185.18, 189.05, 230.03** [IMAGE AVAILABLE]

43. 5,345,424, Sep. 6, 1994, Power-up reset override architecture and circuit for **flash memory**; Marc Landgraf, **365/227, 218** [IMAGE AVAILABLE]

44. 5,333,122, Jul. 26, 1994, Electrically erasable and programmable non-volatile semiconductor memory device having word line voltage control circuit using internal voltage booster circuit; Kazuhisa Ninomiya, **365/189.11, 185.22, 185.23, 185.33, 189.06, 189.09** [IMAGE AVAILABLE]

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46. 5,311,466, May 10, 1994, FLASH-EPROM with enhanced immunity from soft-programming of reference cells; Virginia Natale, et al., **365/185.23, 182, 185.02, 185.09, 185.2, 185.26, 185.33, 210** [IMAGE AVAILABLE]

47. 5,293,560, Mar. 8, 1994, Multi-state flash EEPROM system using incremental programing and erasing methods; Eliyahou Harari, **365/185.03, 185.09, 185.11, 185.19, 185.2,**

185.22, **185.3**, **189.07**, **218**, **230.03** [IMAGE AVAILABLE]

48. 5,263,000, Nov. 16, [redacted]3, Drain power supply; Michael A. [redacted] Buskirk, et al., **365/185.33**, **227** [IMAGE AVAILABLE]

49. 5,237,535, Aug. 17, 1993, Method of repairing overerased cells in a **flash memory**; Neal Mielke, et al., **365/185.3**, **185.12**, **185.19**, **185.21**, **185.22**, **185.24**, **200** [IMAGE AVAILABLE]

50. 5,199,032, Mar. 30, 1993, Microcontroller having an EPROM with a low voltage program inhibit circuit; Robert W. Sparks, et al., **371/3**; 364/240, 240.2, 241.9, 244, 244.3, 244.6, 247, 247.8, 259, 259.1, 259.2, 273, 273.4, 707, DIG.1; **395/182.01** [IMAGE AVAILABLE]

51. 5,172,338, Dec. 15, 1992, Multi-state EEprom read and write circuits and techniques; Sanjay Mehrotra, et al., **365/185.03**, **184**, **185.33**, **189.07**, **195**, **201** [IMAGE AVAILABLE]

52. 5,163,021, Nov. 10, 1992, Multi-state EEprom read and write circuits and techniques; Sanjay Mehrotra, et al., **365/185.03**; 330/2; **365/104**, **168**, **185.22**, **189.09**, **201** [IMAGE AVAILABLE]

53. 5,008,566, Apr. 16, 1991, Power supply voltage drop detection circuit for use in **EEPROM memory**; Kiyokazu Hashimoto, 327/543, 546, 566, 581; **365/228** [IMAGE AVAILABLE]

54. 5,003,510, Mar. 26, 1991, Semiconductor **memory** device with **flash** write mode of operation; Sachiko Kamisaki, **365/189.01**, **189.05**, **230.03** [IMAGE AVAILABLE]

55. 4,771,399, Sep. 13, 1988, Method and apparatus for programming memory through battery terminals; Gregory O. Snowden, et al., **365/226**; 340/825.44; 364/DIG.1, DIG.2; 455/186.2; **711/103** [IMAGE AVAILABLE]

56. 4,733,394, Mar. 22, 1988, Electrically programmable semiconductor memory showing redundance; Burkhard Giebel, **371/10.3**; **365/201**; **371/21.2** [IMAGE AVAILABLE]

57. 4,612,632, Sep. 16, 1986, Power transition write protection for PROM; Anthony M. Olson, **365/226**, **228**; **395/182.2** [IMAGE AVAILABLE]

58. 4,608,585, Aug. 26, 1986, Electrically erasable PROM cell; Parviz Keshtbod, 257/321, 322; **365/185.1**, **185.29** [IMAGE AVAILABLE]

US PAT NO: 5,008,566 [IMAGE AVAILABLE] L12: 53 of 58
TITLE: Power supply voltage drop detection circuit for use in **EEPROM memory**
US-CL-CURRENT: 327/543, 546, 566, 581; **365/228**

SUMMARY:

BSUM(8)

Therefore, . . . or a power supply voltage drops down below a tolerable level due to a trouble of a system incorporating the **EEPROM** therein, a **memory** cell in the EEPROM is erroneously written or erased. In the above table, for example, when the EEPROM is in. . . power supply voltage drops, a voltage applied to the CE terminal is brought from the high level to a low **level** and a **voltage** applied to the OE terminal is also brought from the high level to a low level. At this time, assuming. . .

CLAIMS:

CLMS(1)

I . . .

drain connected to a power supply voltage line and a gate connected to ground, said first N-channel field-effect-transistor having a **threshold** whose absolute **value** has a positive temperature characteristic, a second N-channel field-effect-transistor having a drain connected to a source of the first N-channel. . . and a gate connected to a connection node between the first and second N-channel field-effect-transistors, said P-channel field-effect-transistor having a **threshold** whose absolute **value** has a negative temperature characteristic, a third N-channel field-effect-transistor having a drain connected to a drain of the P-channel field-effect-transistor. . . third N-channel field-effect-transistor and having an output generating a signal which is a function of the sum of the absolute **value** of the **threshold** of the first N-channel field-effect-transistor and the absolute **value** of the **threshold** of the P-channel field-effect-transistor and indicative of a power supply voltage drop.

CLAIMS:

CLMS(4)

4. . . .
and fourth field-effect-transistors and having an output generating a signal which is a function of the sum of the absolute **value** of the **threshold** of the first field-effect-transistor and the absolute **value** of the **threshold** of the third field-effect-transistor and indicative of a power supply voltage drop.

US PAT NO: 5,003,510 [IMAGE AVAILABLE] L12: 54 of 58
TITLE: Semiconductor **memory** device with **flash** write mode of operation
US-CL-CURRENT: **365/189.01, 189.05, 230.03**

SUMMARY:

BSUM(9)

When the single bit write mode operation is established in the semiconductor **memory** device, the **flash** write mode selecting signal FWM remains in the inactive high **voltage level**, so that the NAND gates serve as inverter circuits to produce the complementary signals of the output signals of the. . . the semiconductor memory

device, the controlling unit 10 shifts the flash write mode selecting signal FWM to the active [redacted] **voltage level**, so that all of the NAND gates 23 to 27 produ[redacted] the output signals of the high vo[redacted]**ge level** regardless of the output signals from the decoder section 21. Then, all of the switching units of the column switch. . .

CLAIMS:

CLMS(1)

What . . .
to the memory cells of the columns, respectively, and operative to propagate data bits in the form of differences in **voltage level**, respectively, said bit line pairs having first bit lines respectively paired with second bit lines;
(d) a row addressing facility supplied. . . sense amplifier circuits respectively coupled to the bit line pairs and responsive to activation signals for increasing the differences in **voltage level**, thereby quickly deciding the logic levels of said data bits;
(f) an input-and-output data facility supplied with a single write data. . . coupled to said input-and-output data facility for propagating the single write data bit in the form of a difference in **voltage level** in the single bit write mode of operation;
(h) a flash write data bus system coupled to said input-and-output data facility for propagating the flash write data bit in the form of either high or low **voltage level** in the flash write mode of operation;
(i) a column addressing facility supplied with column address bits and operative to produce. . .

US PAT NO: 4,771,399 [IMAGE AVAILABLE] L12: 55 of 58
US-CL-CURRENT: **365/226**; 340/825.44; 364/DIG.1, DIG.2; 455/186.2; **711/103**

ABSTRACT:
A . . . programming and reading an electronic device memory through its power source connections. Circuitry is provided for programming and reading internal **EEPROM memory** of a portable radio with information provided by an external programming apparatus through its existing battery terminals, wihout removing the. . .

DETDESC:

DETD(10)

During . . . controls the application of the programming voltage to device memory 128 in response to information obtained from the different programming **voltage levels**. The sequence of programming steps performed by device controller 126 will be discussed in the description accompanying FIG. 4. Device. . . combined with the existing electronic device microcomputer through the use of a PROM-programming subroutine. Device memory 128 is the existing **EEPROM memory** of electronic device 120.

CLAIMS:

CLMS(7)

7. The programming method according to claim 6, wherein said voltage modulating step is performed by varying the DC **voltage level** of said substitute power signal in digital steps at a rate corresponding to said program data and at a level above the nominal **voltage level** of said electronic device power source.

CLAIMS:

CLMS(19)

19. The memory programming system according to claim 18, wherein said voltage modulating means varies the DC **voltage level** of said substitute power signal in digital steps at a rate corresponding to said program data and at a level above the nominal **voltage level** of said electronic device power source.

CLAIMS:

CLMS(26)

26. . . .
to said radio memory; and
(g) controlling the programming operation of said radio memory in response to said programming signal DC **voltage levels** and said serial program data, whereby said radio internal memory is programmed by said external programming apparatus through said radio. . .

CLAIMS:

CLMS(32)

32. The programming method according to claim 31, wherein said voltage modulating step is performed by varying the DC **voltage level** of said substitute voltage in digital steps at a rate corresponding to said serial program data and at a level above the nominal **voltage level** of said radio battery.

CLAIMS:

CLMS(34)

34. . . . step of measuring the current drain of said portable radio before said substitute voltage is raised to its final programming **voltage level**.

CLAIMS:

CLMS(41)

41. . . .
said radio memory; and
means for controlling the programming operation of said radio memory in response to said programming signal DC **voltage levels** and said serial program data, whereby said radio internal memory is programmed by said external programming apparatus through said radio. . .

CLAIMS:

CLMS(45)

45. The memory programming system according to claim 44, wherein said voltage modulating means varies the DC **voltage level** of said substitute voltage in digital steps at a rate corresponding to said serial program data and at a level above the nominal **voltage level** of said radio battery.

CLAIMS:

CLMS(47)

47. . . . means for measuring the current drain of said portable radio before said substitute voltage is raised to its final programming **voltage level**.

US PAT NO: 4,733,394 [IMAGE AVAILABLE] L12: 56 of 58
US-CL-CURRENT: **371/10.3; 365/201; 371/21.2**

ABSTRACT:
An integrated memory system includes a microcomputer which, at defined intervals and by employing a classifying circuit integrated in an **EEPROM**, checks the **memory** cells of the EEPROM with respect to variations of the **threshold values**. Upon detection of a fault in a row or column which has thus been recognized as being faulty, this faulty. . .

CLAIMS:

CLMS(2)

2. . . .
said matrix;

storing predetermined data in rows of said matrix;
reading each row of said memory a plurality of times;
providing a reference voltage level from a reference voltage cell;
comparing the output voltage level of each cell of a row with said reference voltage level from said reference voltage cell to detect defective rows;
varying said reference voltage level for each time a row is read out to detect defective rows;
storing the address of a defective row in one. . .

US PAT NO: 4,612,632 [IMAGE AVAILABLE] L12: 57 of 58
US-CL-CURRENT: **365/226, 228; 395/182.2**

ABSTRACT:
A . . . transition detection and override circuit is coupled to the OUTPUT-ENABLE (OE) pin of a nonvolatile electrically erasable programmable read only **memory** (**EEPROM**) for preventing inadvertent write commands thereto from a microprocessor arising from supply voltage (V.sub.cc) transitions, including power up and power. . .

CLAIMS:

CLMS(1)

I claim:

1. For use with a nonvolatile electrically erasable programmable read only **memory** (**EEPROM**) and a microprocessor coupled by means of a bi-stable OUTPUT-ENABLE control line wherein the microprocessor provides an enable signal via. . . in a second state, said EEPROM and said microprocessor further coupled to a power supply and energized by a predetermined **voltage level** therefrom, a circuit for preventing the inadvertent writing of data by the microprocessor into the EEPROM when the supply voltage drops below said predetermined **voltage level**, said circuit comprising:
supply voltage detection means including means for generating said predetermined **voltage level** and **voltage** comparison means coupled thereto and to the power supply and responsive to the supply voltage therefrom for comparing the supply voltage with said predetermined **voltage level** and for generating a control signal when the supply voltage drops below the predetermined **voltage level**; and
control means coupled to the OUTPUT-ENABLE control line and to said supply voltage detection means and responsive to said control. . . microprocessor and maintaining the OUTPUT-ENABLE control line in said first state when the supply voltage is less than the predetermined **voltage level** in preventing the inadvertent writing of data by the microprocessor into the EEPROM with variations in the supply voltage of. . .

CLAIMS:

CLMS(2)

2. The circuit of claim 1 wherein said predetermined **voltage level** is approximately 4.75 VDC.

CLAIMS:

CLMS(5)

5. . . . means for preventing the writing of data therein from the microprocessor if said supply voltage is less than a designated **voltage value**, wherein said designated **voltage value** is less than the predetermined **voltage level**.

CLAIMS:

CLMS(6)

6. The circuit of claim 1 wherein said supply voltage detection means includes means for generating said predetermined **voltage level** and **voltage** comparison means coupled thereto and to the power supply

for comparing the supply voltage with said predetermined **voltage level** and for generating [redacted]d control signal when the supply v[redacted]tage drops below the predeterm[redacted]d **voltage level**.

US PAT NO: 4,608,585 [IMAGE AVAILABLE] L12: 58 of 58
US-CL-CURRENT: 257/321, 322; **365/185.1, 185.29**

ABSTRACT:
In an **EEPROM memory** cell of the kind which relies on tunneling action through a thin oxide layer to store charge on a floating. . . the substrate is greatly reduced during erase mode. As a result, little or no tunneling occurs during programming and the **threshold voltage level** is the same as the virgin **threshold value** of the memory cell. However, during erase, very efficient tunneling occurs from the floating gate to the substrate and the **threshold voltage level** decreases to a negative value. The difference between positive and negative **values** of the **threshold** voltage is comparable to that of conventional memory cells.

102. 4,377,857, Mar. 22, 1983, Electrically erasable programmable read-only memory; Andrew C. Tickle, 365/185.33; 257/321; 365/182, 185.02, 185.06, 185.18, 185.25, 185.26 [IMAGE AVAILABLE]

US PAT NO: 4,377,857 [IMAGE AVAILABLE] L4: 102 of 104

ABSTRACT:
An electrically erasable programmable read-only memory (E.sup.2 PROM) is provided which utilizes an inhibit voltage applied to unselected word lines during writing to prevent writing in unselected rows. In the preferred embodiment, each memory cell of the E.sup.2 PROM array consists of a single floating gate field effect transistor. The E.sup.2 PROM of the present invention provides for row erasure and single bit writing.

CLAIMS:

CLMS(11)

11. An electrically erasable **programmable** read-only memory comprising:
(a) a memory array comprising
(i) a matrix of memory cells formed as a plurality of rows and a plurality of columns of said cells, each of said cells utilizing a **floating gate** field effect transistor for storage of binary data;
(ii) a plurality of word lines, the control gate of each said transistor in a row of said memory cells being connected to a word line corresponding to said row;
(iii) a plurality of bit lines, the drain of each said transistor in a column of said memory cells being connected to a bit line corresponding to said column; and
(iv) a plurality of source lines, the source of each said transistor in a column of said memory cells being connected to a source line corresponding to said column;
(b) a row address decoder having a plurality of output lines, individual of said output lines being connected to a corresponding of said word lines, comprising
(i) means for directing an erase **voltage** to a selected output line while simultaneously maintaining unselected output lines at zero potential;
(ii) means for maintaining a selected output line at zero potential and simultaneously directing an inhibit **voltage** which is less than said erase **voltage** to unselected output lines; and
(iii) means for applying a read **voltage** to a selected output line and simultaneously maintaining unselected output lines at zero potential;
(c) a column address decoder having a plurality of output lines, individual of said output lines being connected to a corresponding of said bit lines, comprising
(i) means for maintaining all of said bit lines at zero potential;
(ii) means for applying a write **voltage** to selected of said bit lines and simultaneously maintaining unselected bit lines at zero potential; and
(iii) means for applying a small potential to selected of said bit lines and simultaneously maintaining unselected bit lines at zero potential; and
(d) an input/output buffer connected to said memory array for **determining** whether selected of said memory cells of said array are conducting or nonconducting.

95. 4,663,740, May 5, 1987, High speed eprom cell and array; Mark S. Ebel, 365/185.1; 257/316; 365/178, 185.06, 185.24 [IMAGE AVAILABLE]

US PAT NO: 4,663,740 [IMAGE AVAILABLE] L4: 95 of 104

ABSTRACT:
A high speed EPROM cell comprises two floating gate field effect transistors and one field effect transistor. One of the floating gate transistors is smaller than the other floating gate transistor and functions as a programming transistor in developing charge on the interconnected floating gates. The larger dimensions of the other floating gate transistor allows increased read current and operating speed. The field effect transistor connects the larger floating gate transistor to a read drain terminal. The cell is readily fabricated using two doped polycrystalline semiconductor lines and two metallization lines in accordance with conventional semiconductor processing techniques.

CLAIMS:

CLMS(11)

11. An EPROM cell comprising a first **floating gate** field effect transistor and a second **floating gate** field effect transistor, said first transistor being smaller than said second transistor, means electrically connecting the floating gates of said first and second transistors, a write terminal connected to gates of said first and second transistors, a **programming voltage** terminal connected to apply a **programming voltage** to said first transistor, a third field effect transistor serially connected with said second transistor for **determining** the **programmed** conductivity of said second transistor, and a read terminal connected through said third transistor to said second transistor.

94. 4,718,041, Jan. 5, 1988, EEPROM memory having extended life; David A. Baglee, et al., 365/185.22, 185.09, 185.1, 185.29, 222 [IMAGE AVAILABLE]

US PAT NO: 4,718,041 [IMAGE AVAILABLE] L4: 94 of 104

ABSTRACT:
Disclosed is a method and apparatus for extending the programmable life of an EEPROM memory. For each write commamd generated external to the memory an automatic internal read operation is executed. Each internally generated read operation is accompanied by an increased sense voltage. Data written into selected cells is temporarily stored and compared with the data read. If a match of the compared data is found, the memory operations continue as usual. If a mismatch is found, an internally generated write operation is generated, the programming voltage is increased, and the data temporarily stored is rewritten at the increased voltage. Data polling features are provided with both the internal and externally generated write operations.

CLAIMS:

CLMS(19)

19. Circuitry for extending the **programmable** life of an **EEPROM** memory of the type having a plurality of **floating gate** storage cells, comprising:
means for writing data into the cells of the memory in response to an externally generated write command;
means for reading data from the cells of the memory in response to an externally generated read command;
means responsive to said write command for temporarily storing the data to be written in the memory cells while also writing said data into said memory cells in response to the external write command;
said means for reading including means for generating a variable sense **voltage** for use in **determining** whether data read from the memory cells is a one or a zero;
means for increasing the sense **voltage** and for reading the memory cells which were written in response to said external write command;
means for comparing the data temporarily stored with the data read as a result of the internal read operation, and for providing match and mismatch indications thereof;
means for applying a variable **programming voltage** to said cells; and
means for increasing the **programming voltage** and means for writing the temporarily stored data into said memory cells in response to a mismatch indication from said comparing means.

1. 5,719,808, Feb. 17, 1998, Flash **EEPROM** system; **Eliyahou Harari**, et al., 365/185.33, 185.22, 185.29 [IMAGE AVAILABLE]

2. 5,712,819, Jan. 27, 1998, Flash **EEPROM** system with storage of sector characteristic information within the sector; **Eliyahou Harari**, 365/185.29, 185.24, 185.3, 185.33, 218 [IMAGE AVAILABLE]

3. 5,693,570, Dec. 2, 1997, Process for manufacturing a programmable power generation circuit for flash **EEPROM** memory systems; Raul-Ardian Cernea, et al., 1/1 [IMAGE AVAILABLE]

4. 5,671,229, Sep. 23, 1997, Flash **eeprom** system with defect handling; **Eliyahou Harari**, et al., 371/10.2; 365/200; 395/182.01, 182.03 [IMAGE AVAILABLE]

5. 5,663,901, Sep. 2, 1997, Computer memory cards using flash **EEPROM** integrated circuit chips and memory-controller systems; Robert F. Wallace, et al., 365/52, 185.11, 185.33; 395/500; 711/103 [IMAGE AVAILABLE]

6. 5,659,550, Aug. 19, 1997, Latent defect handling in **EEPROM** devices; **Sanjay Mehrotra**, et al., 371/21.4, 10.3 [IMAGE AVAILABLE]

7. 5,657,332, Aug. 12, 1997, Soft errors handling in **EEPROM** devices; Daniel L. Auclair, et al., 371/40.11; 365/184, 189.07, 189.11; 371/21.4 [IMAGE AVAILABLE]

8. 5,654,217, Aug. 5, 1997, Dense flash **EEPROM** cell array and peripheral supporting circuits formed in deposited field oxide with the use of spacers; Jack H. Yuan, et al., 438/588; 257/320; 438/258, 266, 593, 594 [IMAGE AVAILABLE]

9. 5,642,312, Jun. 24, 1997, Flash **EEPROM** system cell array with more than two storage states per memory cell; **Eliyahou Harari**, 365/185.03, 185.18, 185.19, 185.24, 185.28, 185.29 [IMAGE AVAILABLE]

10. 5,621,685, Apr. 15, 1997, Programmable power generation circuit for flash **EEPROM** memory systems; Raul-Adrian Cernea, et al., 365/185.18, 185.33 [IMAGE AVAILABLE]

11. 5,602,987, Feb. 11, 1997, Flash **EEprom** system; **Eliyahou Harari**, et al., 395/182.06; 365/200, 210; 711/100 [IMAGE AVAILABLE]

12. 5,596,532, Jan. 21, 1997, Flash **EEPROM** self-adaptive voltage generation circuit operative within a continuous voltage source range; Raul-Adrian Cernea, et al., 365/185.18, 185.33, 189.07, 226 [IMAGE AVAILABLE]

13. 5,592,420, Jan. 7, 1997, Programmable power generation circuit for flash **EEPROM** memory systems; Raul-Adrian Cernea, et al., 365/185.18, 185.33, 189.09, 226 [IMAGE AVAILABLE]

14. 5,583,812, Dec. 10, 1996, Flash **EEPROM** system cell array with more than two storage states per memory cell; **Eliyahou Harari**, 365/185.33, 182, 185.03, 185.18, 185.19, 185.22, 185.24 [IMAGE AVAILABLE]

15. 5,568,439, Oct. 22, 1996, Flash **EEPROM** system which maintains individual memory block cycle counts; **Eliyahou Harari**, 365/185.09, 185.18, 185.19, 185.22, 185.27, 185.29, 185.3, 185.33 [IMAGE AVAILABLE]

16. 5,568,424, Oct. 22, 1996, Programmable power generation circuit for flash **EEPROM** memory systems; Raul-Adrian Cernea, et al., 365/185.33, 185.18, 226 [IMAGE AVAILABLE]

17. 5,563,825, Oct. 8, 1996, Programmable power generation circuit for

flash **eeprom** memory systems; Raul-Adrian Cernea, et al., 365/185.18; 327/536; 365/185.23, 185.[redacted] 189.09, 226 [IMAGE AVAILABLE]

18. 5,554,553, Sep. 10, 1996, Highly compact EPROM and flash **EEPROM** devices; **Eliyahou Harari**, 438/264; 257/298, 320; 365/185.26, 185.33; 438/266, 588, 594 [IMAGE AVAILABLE]

19. 5,544,118, Aug. 6, 1996, Flash **EEPROM** system cell array with defect management including an error correction scheme; **Eliyahou Harari**, 365/218, 182, 185.29, 185.31, 185.33, 189.09, 200 [IMAGE AVAILABLE]

20. 5,535,328, Jul. 9, 1996, Non-volatile memory system card with flash erasable sectors of **EEprom** cells including a mechanism for substituting defective cells; **Eliyahou Harari**, et al., 395/182.05; 364/268.5, DIG.1; 365/218; 395/182.06, 833; 711/115 [IMAGE AVAILABLE]

21. 5,534,456, Jul. 9, 1996, Method of making dense flash **EEPROM** cell array and peripheral supporting circuits formed in deposited field oxide with sidewall spacers; Jack H. Yuan, et al., 438/263; 257/316; 438/303 [IMAGE AVAILABLE]

22. 5,532,964, Jul. 2, 1996, Method and circuit for simultaneously programming and verifying the programming of selected **EEPROM** cells; Raul-Adrian Cernea, et al., 365/189.09, 185.18, 189.07 [IMAGE AVAILABLE]

23. 5,532,962, Jul. 2, 1996, Soft errors handling in **EEPROM** devices; Daniel L. Auclair, et al., 365/201, 184, 185.02, 185.09, 185.24 [IMAGE AVAILABLE]

24. 5,512,505, Apr. 30, 1996, Method of making dense vertical programmable read only memory cell structure; Jack H. Yuan, et al., 438/264; 148/DIG.50; 438/594 [IMAGE AVAILABLE]

25. 5,508,971, Apr. 16, 1996, Programmable power generation circuit for flash **EEPROM** memory systems; Raul-Adrian Cernea, et al., 365/185.23, 185.14, 185.18, 189.09, 226 [IMAGE AVAILABLE]

26. 5,504,760, Apr. 2, 1996, Mixed data encoding **EEPROM** system; **Eliyahou Harari**, et al., 371/40.11; 365/190 [IMAGE AVAILABLE]

27. 5,495,442, Feb. 27, 1996, Method and circuit for simultaneously programming and verifying the programming of selected **EEPROM** cells; Raul-Adrian Cernea, et al., 365/185.03, 185.14, 185.16, 185.21, 185.22, 194 [IMAGE AVAILABLE]

28. 5,471,478, Nov. 28, 1995, Flash **EEPROM** array data and header file structure; John S. Mangan, et al., 371/10.3; 365/200; 371/10.2 [IMAGE AVAILABLE]

29. 5,438,573, Aug. 1, 1995, Flash **EEPROM** array data and header file structure; John S. Mangan, et al., 371/10.3, 2.1, 21.6 [IMAGE AVAILABLE]

30. 5,434,825, Jul. 18, 1995, Flash **EEPROM** system cell array with more than two storage states per memory cell; **Eliyahou Harari**, 365/185.24, 182, 185.29, 189.07, 218 [IMAGE AVAILABLE]

31. 5,430,859, Jul. 4, 1995, Solid state memory system including plural memory chips and a serialized bus; **Robert D. Norman**, et al., 711/103; 364/DIG.1; 365/52, 185.33, 230.03; 395/500 [IMAGE AVAILABLE]

32. 5,428,621, Jun. 27, 1995, Latent defect handling in **EEPROM** devices; **Sanjay Mehrotra**, et al., 371/21.4, 10.3 [IMAGE AVAILABLE]

33. 5,422,842, Jun. 6, 1995, Method and circuit for simultaneously programming and verifying the programming of selected **EEPROM** cells; Raul-Adrian Cernea, et al., 365/185.22, 185.14, 185.16, 185.21, 185.24 [IMAGE AVAILABLE]

34. 5,418,752, May 23, 1995, Flash **EEPROM** system with erase sector select; **Eliyahou Harari**, et al., 365/218, 185.09, 185.11, 185.22, 185.29 [IMAGE AVAILABLE]

35. 5,396,468, Mar. 7, 1995, Streamlined write operation for **EEPROM**

53. 5,043,940, Aug. 27, [redacted]1, Flash **EEPROM** memory systems hav[redacted] multistate storage cells; **[redacted]iyahou Harari**, 365/185.03, 185.09, [redacted] 185.11, 185.19, 185.2, 185.22, 185.25, 185.3, 185.33, 218 [IMAGE AVAILABLE]

54. 4,998,220, Mar. 5, 1991, **EEPROM** with improved erase structure; Boaz Eitan, et al., 365/185.14; 257/321; 365/51, 185.16, 185.18, 185.3, 185.31, 185.33, 218 [IMAGE AVAILABLE]

55. 4,612,640, Sep. 16, 1986, Error checking and correction circuitry for use with an electrically-programmable and electrically-erasable memory array; **Sanjay Mehrotra**, et al., 371/40.4, 37.03, 40.18 [IMAGE AVAILABLE]

56. 4,612,629, Sep. 16, 1986, Highly scalable dynamic RAM cell with self-signal amplification; **Eliyahou Harari**, 365/185.08; 257/262, 300; 348/307; 365/182, 185.02, 185.03, 185.16, 185.2, 185.25, 185.27, 185.29 [IMAGE AVAILABLE]

57. 4,409,723, Oct. 18, 1983, Method of forming non-volatile EPROM and **EEPROM** with increased efficiency; **Eliyahou Harari**, 438/257; 257/323; 438/263, 264 [IMAGE AVAILABLE]

system; **Eliyahou Harari**, et al., 365/218, 185.01, 189.01 [IMAGE AVAILABLE]

36. 5,380,672, Jan. 10, 1995, Dense vertical programmable read only memory cell structures and processes for making them; Jack H. Yuan, et al., 438/257; 365/185.02, 185.27, 185.31, 185.33; 438/267 [IMAGE AVAILABLE]

37. 5,369,615, Nov. 29, 1994, Method for optimum erasing of **EEPROM**; **Eliyahou Harari**, et al., 365/185.19, 185.09, 185.14, 185.22, 185.31, 185.33 [IMAGE AVAILABLE]

38. 5,343,063, Aug. 30, 1994, Dense vertical programmable read only memory cell structure and processes for making them; Jack H. Yuan, et al., 257/317, 316, 319, 320; 365/185.14, 185.27, 185.33 [IMAGE AVAILABLE]

39. 5,315,541, May 24, 1994, Segmented column memory array; **Eliyahou Harari**, et al., 365/185.13, 51, 185.02, 185.14, 185.16, 185.33 [IMAGE AVAILABLE]

40. 5,297,148, Mar. 22, 1994, Flash **eeprom** system; **Eliyahou Harari**, et al., 371/10.2; 365/185.09, 185.33, 200; 371/10.3; 395/182.05 [IMAGE AVAILABLE]

41. 5,293,560, Mar. 8, 1994, Multi-state flash **EEPROM** system using incremental programing and erasing methods; **Eliyahou Harari**, 365/185.03, 185.09, 185.11, 185.19, 185.2, 185.22, 185.3, 189.07, 218, 230.03 [IMAGE AVAILABLE]

42. 5,270,979, Dec. 14, 1993, Method for optimum erasing of **EEPROM**; **Eliyahou Harari**, et al., 365/185.09, 185.11, 185.14, 185.33, 189.01, 200 [IMAGE AVAILABLE]

43. 5,268,870, Dec. 7, 1993, Flash **EEPROM** system and intelligent programming and erasing methods therefor; **Eliyahou Harari**, 365/185.09, 185.03, 185.19, 185.21, 185.22, 185.25, 185.33, 189.07, 200, 236; 371/10.2, 21.1, 21.4; 711/103 [IMAGE AVAILABLE]

44. 5,268,319, Dec. 7, 1993, Highly compact EPROM and flash **EEPROM** devices; **Eliyahou Harari**, 438/260; 257/320; 438/263, 266, 964 [IMAGE AVAILABLE]

45. 5,268,318, Dec. 7, 1993, Highly compact EPROM and flash **EEPROM** devices; **Eliyahou Harari**, 438/263; 257/320; 365/185.02, 185.03, 185.06, 185.14, 185.16, 185.18, 185.19, 185.26, 185.27, 185.3, 185.33; 438/260, 266, 972 [IMAGE AVAILABLE]

46. 5,200,959, Apr. 6, 1993, Device and method for defect handling in semi-conductor memory; Stephen Gross, et al., 371/21.6; 364/236.2, 238, 240, 244, 244.6, 245.3, 251, 264, 264.5, 265, 280, 280.2, 282.1, 282.3, 285.3, DIG.1; 371/10.2; 395/182.06 [IMAGE AVAILABLE]

47. 5,198,380, Mar. 30, 1993, Method of highly compact EPROM and flash **EEPROM** devices; **Eliyahou Harari** [IMAGE AVAILABLE]

48. 5,172,338, Dec. 15, 1992, Multi-state **EEprom** read and write circuits and techniques; **Sanjay Mehrotra**, et al., 365/185.03, 184, 185.33, 189.07, 195, 201 [IMAGE AVAILABLE]

49. 5,168,465, Dec. 1, 1992, Highly compact EPROM and flash **EEPROM** devices; **Eliyahou Harari**, 257/320, 321; 365/185.03, 185.09, 185.14, 185.15, 185.22, 185.25, 185.27, 203 [IMAGE AVAILABLE]

50. 5,163,021, Nov. 10, 1992, Multi-state **EEprom** read and write circuits and techniques; **Sanjay Mehrotra**, et al., 365/185.03; 330/2; 365/104, 168, 185.22, 189.09, 201 [IMAGE AVAILABLE]

51. 5,095,344, Mar. 10, 1992, Highly compact EPROM and flash **EEPROM** devices; **Eliyahou Harari**, 257/328, 327, 488; 365/185.03, 185.09, 185.19, 185.2, 185.22, 185.27, 185.3, 185.31, 185.33 [IMAGE AVAILABLE]

52. 5,070,032, Dec. 3, 1991, Method of making dense flash **EEprom** semiconductor memory structures; Jack H. Yuan, et al., 438/267, 527, 588, 594 [IMAGE AVAILABLE]

93. 4,785,424, Nov. 15, 1988, Apparatus for page mode programming of an EEPROM cell array with false loading protection; Tien-Ler Lin, et al., 365/185.25, 185.21, 204, 238.5 [IMAGE AVAILABLE]

US PAT NO: 4,785,424 [IMAGE AVAILABLE] L4: 93 of 104

ABSTRACT:
An apparatus for page mode programming of a memory cell with false loading protection is disclosed. The apparatus discharges any residual voltage left on the bit line after a read operation to prevent this voltage from being erroneously loaded into temporary storage apparatus associated with the bit line. In a preferred embodiment, two transistors are placed in series between the bit line and the array V.sub.ss line. A first transistor is controlled by a signal indicating that information is to be loaded into the temporary storage apparatus. The second transistor is controlled by a signal indicating that no memory cell associated with the bit line has been selected for programming.

CLAIMS:

CLMS(1)

What is claimed is:

1. An apparatus for page mode **programming** of an **EEPROM** memory cell array comprising:
a bit line associated with a plurality of memory cells,
temporary storage means, operatively connected to said bit line, for storing information to be **programmed** into a memory cell associated with said bit line,
means for **determining** when no **EEPROM** memory cell associated with said bit line has been selected form **programming** during a page mode **programming** cycle, and
means for discharging **voltage** on said bit line during a loading cycle of said temporary storage means during said page mode **programming** cycle when no **EEPROM** memory cell associatd with said bit line has been selected for **programming**.

CLAIMS:

CLMS(2)

2. An apparatus for page mode **programming** of an **EEPROM** memory cell array with false loading prevention, comprising:
a bit line, operatively connected to a plurality of memory cells,
temporary storage means, operatively connected to said bit line, for storing information to be loaded into said memory cells,
means for **determining** when no memory cell operatively connected to said bit line has been selected for **programming** during a page mode **programming** cycle,
means for discharging **voltage** on said bit line during a loading cycle for said temporary storage means when no memory cell operatively connected to said bit line has been selected for **programming** during said page mode **programming** cycle, and
a high **voltage** source, operatively connected to said bit line, for raising the **voltage** of said bit line at a selected time during said page mode **programming** cycle, said high **voltage** source being electrically connected to said bit line at a selected time only when said temperarty storage means is storing data indicating that a zero is to be **programmed** into one of said memory cells.

L1	5789	S	((EEPROM OR FLASH) (2A) MEMORY)
L2	138440	S	(VOLT? OR THRESHOLD) (2A) (LEVEL# OR VALUE#)
L3	353	S	L1 (P) L2
L4	274	S	L3 AND (395 OR 365 OR 371 OR 711)/CLAS
L5	683	S	L1/TI,AB
L6	121	S	L4 AND L5
L7	39097	S	L2/AB,CLM
L8	58	S	L6 AND L7